

Overview

Modern systems increasingly rely on ultra-high-speed communication links operating at upper mmWave and terahertz frequencies across advanced silicon interconnect fabrics, silicon photonics, chipllets, and heterogeneous 3DIC architectures. Traditional parasitic extraction flows focus primarily on RC extraction and fail to accurately capture critical electromagnetic effects including:

- Interconnect propagation effects
- EM coupling and isolation
- Frequency-dependent inductive elements
- Current return path interactions
- Substrate and conductor losses
- Full-wave coupling between passive structures

As operating frequencies scale beyond conventional RF ranges, these missing EM effects can significantly impact signal integrity, isolation, and overall system reliability.

What is xLEM™?

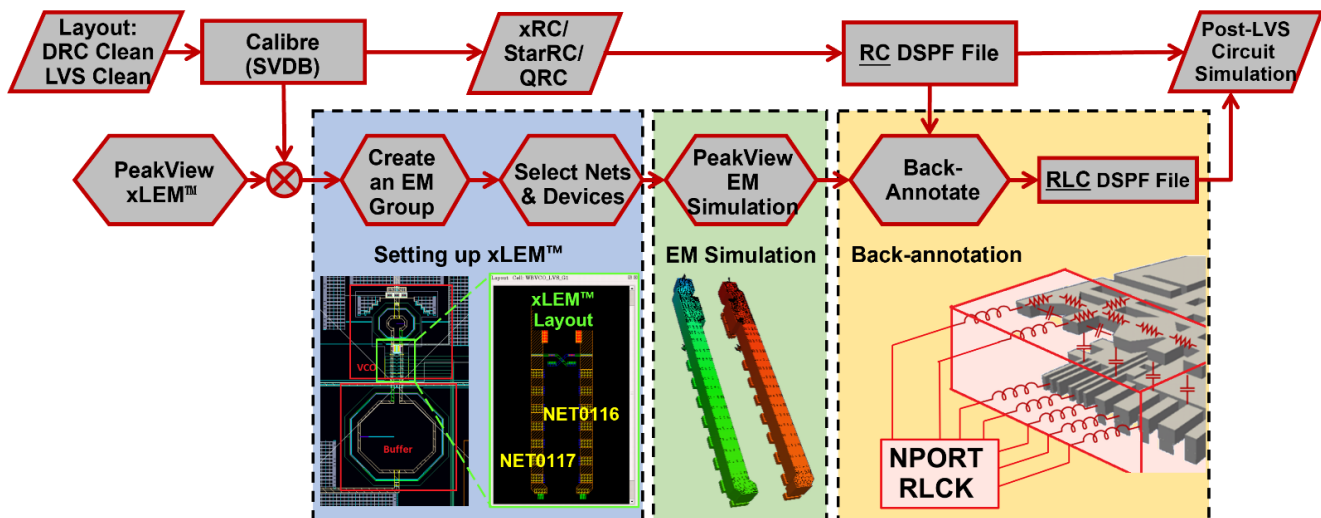
PeakView® xLEM™ is an automated chip-level electromagnetic (EM) extraction and sign-off platform that extends traditional parasitic extraction methodologies into **large-scale 3D full-wave EM extraction**. xLEM™ enables designers to perform physically reliable EM sign-off and EM isolation analysis directly on complete post-LVS layouts while preserving LVS integrity across any hierarchy level. Unlike conventional manual EM workflows, xLEM™ automatically extracts, simulates, models, and back-annotates critical interconnects and passive structures into the post-LVS simulation environment.

xLEM™ Flow:

- EM layout loaded from Calibre-LVS database (SVDB) with automatic port definition and net/passive selection by names.
- EM simulation leverages PeakView® 3D fullwave EM solver technologies.
- Advanced back-annotation automatically connects NPORT and lumped RLCK models to industry-standard parasitic extraction formats.
- EM sign-off with post-LVS circuit simulation including xLEM™ models.

Key Benefits

- **True Chip-Level EM Sign-Off**
Automatic fullwave EM extraction and verification of critical interconnects and passive structures across complete IC, custom silicon, silicon photonics, and 3DIC layouts.
- **Automation & No Manual Rework**
Eliminates manual EM model preparation, black-box partitioning, schematic redesigns, and complex port management workflows.
- **Preserves LVS Integrity**
Works directly on post-LVS verified layouts while maintaining hierarchy and design consistency throughout the EM sign-off flow.
- **Physically Reliable EM Isolation**
Captures realistic current return paths and fullwave coupling effects essential for accurate EM isolation analysis in ultra-high-speed systems.
- **DC to Terahertz Accuracy**
PeakView®'s advanced 3D full-wave EM technology accurately models inductive, resistive, capacitive, and substrate effects from DC through mmWave and terahertz frequencies.



Leveraging PeakView® xLEM™ Sign-Off Flow over Manual Hybrid EM Method

Traditional EM verification flows rely on manually isolating interconnects and passive structures as black-box EM models, requiring extensive schematic and layout redesigns, manual port connections, and incomplete layouts that fail to capture realistic current return paths and full-wave coupling effects. PeakView® xLEM™ replaces this fragmented methodology with a fully automated chip-level **EM extraction and back-annotation flow that preserves LVS integrity across hierarchical designs** while enabling physically reliable 3D full-wave EM sign-off.

	Manual Flow LPE (RC) + EM Model	PeakView xLEM™ Flow LPE (RC) + xLEM™ Extraction/Backannotation
Manual Vs Automated	<ul style="list-style-type: none"> - Manual and inefficient workflow - Requires schematic/layout redesign for EM - No support across hierarchies 	<ul style="list-style-type: none"> - Fully automated EM extraction and backannotation - No need for schematic/redesign - Automated GUI, command line and scripting - Automatic black-box recognition of active devices
Reliability	<ul style="list-style-type: none"> - LVS check "cheated" for EM purposes - Manual connection of hundreds of ports 	<ul style="list-style-type: none"> - LVS-clean layout loading for enhanced reliability - Automated connection of up to thousands of ports
Accuracy and Flexibility	<ul style="list-style-type: none"> - High risk of double-counting parasitic elements - No parasitic L mode 	<ul style="list-style-type: none"> - No double counting and no missing parasitic elements - Multiple modes: parasitic L mode, 2.5D and 3D fullwave. - Support for large-scale and hierarchical schematics
EM Capability	<ul style="list-style-type: none"> - EM tool limit: port number limit, mesh control limit, simulation capacity limit, and accuracy limit 	<ul style="list-style-type: none"> - Unlimited number of ports. High-Capacity Solver - Flexible Mesh Setup for nets and devices - DC-mmWave-TeraHz and 3D fullwave - 3D visualization, post-processing and circuit properties

Flexible Backannotation Methods

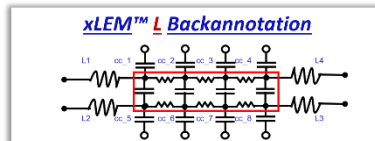
Multiple methodologies support a wide range of high-speed IC, silicon photonics, and 3DIC verification requirements. Designers can select the optimal balance between EM accuracy, simulation capacity, and circuit integration.

xLEM™L extracts frequency-aware parasitic inductive elements directly into the post-LVS netlist while preserving LVS integrity and existing RC extraction data.

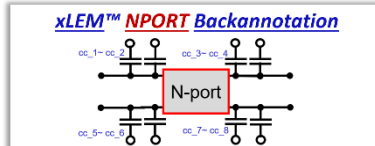
xLEM™NPORT generates broadband full-wave EM models for critical interconnects and passive structures using PeakView®'s 3D EM engine.

Silicon-Correlated Accuracy

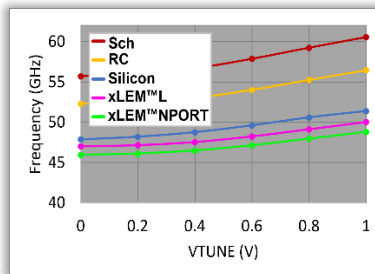
PeakView® EM solver technology has demonstrated strong correlation to silicon measurements across advanced process nodes and high-frequency designs. xLEM™ enables highly reliable EM sign-off for advanced interconnects, silicon photonics, and ultra-high-speed custom silicon systems.



- RC elements are maintained from LPE
- Inductive elements are calculated from PeakView® fullwave simulations



- RC elements are maintained from LPE
- Critical interconnect's RC elements are replaced by an NPORT file from PeakView® fullwave simulations



Standard Format Support

xLEM™ Setup

- iRCX and ITF technology file format from foundries

xLEM™ Input

- Calibre LVS® clean design through SVDB database
- PEX: parasitic extraction results in DSPF file format
- PEX: parasitic extraction results in extracted view format

xLEM™ Output

- n-port, RLCK models
- DSPF file format, backannotated by PeakView® and ready for circuit simulation
- Extracted view, backannotated by PeakView® and ready for circuit simulation