LORENTZ SOLUTION

PeakView PLX
Parasitic Inductance Extraction

Overview

Post Layout Parasitic Extraction has always been an indispensable part of IC design flow, especially with the ever increasing demand of data, speed and performance. Frequencies has surged from RF, mmWave to terahertz, where the traditional RC centric parasitic extraction should be replaced with RLC based parasitic data, in fact, the parasitic inductance impact on top level metals such as signal overshoot and ringing will increase along with the operating frequency, hence it should no longer be ignored and needed to take into considerations to understand the impact on overall circuit or system performance.

Peakview PLX™ is our new parasitic inductance extraction feature based on Peakview's well known 3D Full-wave EM solver which produces silicon matched models across frequencies, it uses proprietary high capacity volume meshing technology to conquer maxwell equations with speed, capacity, and accuracy tuned at 100x improvements for parasitic inductance extraction with no compromise. Net based parasitic inductance values are well modeled hence annotated to today's popular RC extraction flow and results such as DSPF file.

PLX™ Flow Through traditional RC extraction flow, upon the completion of LVS, PEX tools are deployed to extract the interconnect parasitic RCs, and the RC network will be commonly stored in either DSPF file or extracted view. With the new Peakview PLX, the interconnect geometries can be processed by Peakview's superior solver to model the perspective parasitic inductance values, while most importantly, these models will be back annotated to the preserved RC network of the extracted view or DSPF file in the most accurate and compact format, hence producing a complete RLC parasitic network that's ready for post layout simulation.

Benefits

Inductance Extraction Based on Full-wave Simulation Accuracy
PLX is the only parasitic inductance extraction tools based on PeakView's outstanding 3D full-wave simulation.

**Excellent performance & capacity advantage**
PLX is superiorly tuned with 100x performance and capacity wins with outputs accounts for mutual and self-inductance in the most compact form.

PEX Integration & back-annotation
PeakView PLX can be used in stand-alone or within schematic and layout tools to interface with RC extraction flows to produce the complete parasitic RLC network in DSPF format. PLX manages all the details for the back-annotation to ensures data integrity that's for circuit simulations.

Production Proven
The core technologies of PeakView PLX have been in production use for a wide range of RFIC and high speed circuit design for 10+ years, it accounts for skin effect losses missed by traditional RC extraction tools. This makes PLX highly trustworthy for millimeter-wave and beyond integrated system designs.
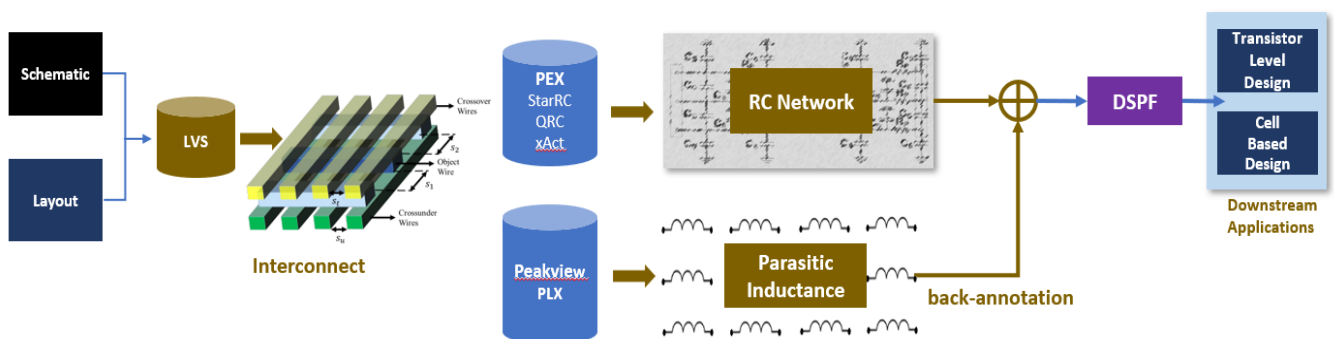
PLX™ Result with Silicon Correlation The post PLX simulations can accurately capture the parasitic influences from DC to 60 GHz and beyond yet demonstrate an excellent correlation to silicon data in advanced process nodes. It's targeted for high-frequency, RF and mixed-signal IC designers to be considered as the most reliable and efficient parasitic inductance extraction tool to date. It can also be deployed for the design and verification of broadband applications of gigabits per second (Gbps) on-chip communication systems. Full-scale implementation of PLX in the PEX flow will greatly facilitate research and development in the 5G (5th Generation wireless network) standards and associated hardware, where millimeter wave frequency bands are of primary interest.

Sample: Comparison of output frequency in Mode 4
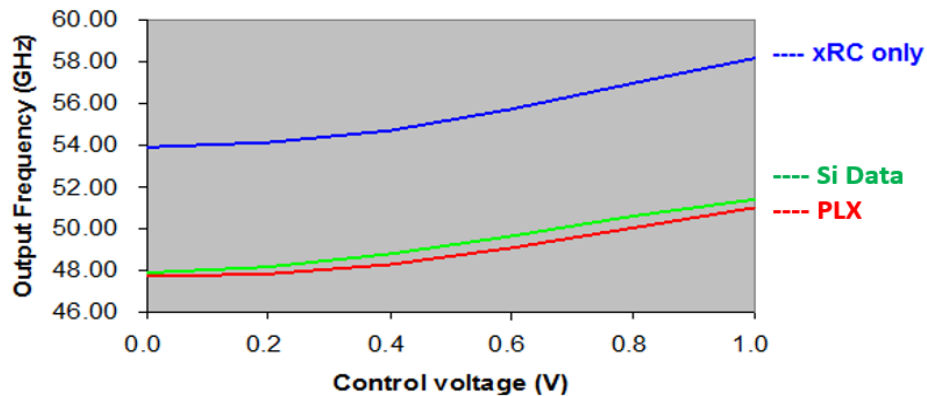
Multi-mode 50 GHz VCO output frequency comparison

PeakView™ electromagnetic design platform offers the most comprehensive design solution covering every EM design needs across every design stage for today's most challenging RF/mmWave/TeraHz High Speed IC design applications. Backed by the industry proven 3D Full-wave EM solver as the foundation core and extended to a variety of solutions such as passive device synthesis and modeling. PeakView is now offering the capability to perform parasitic inductance extraction that complements today's most commonly deployed RC extraction tools in DSPF format.
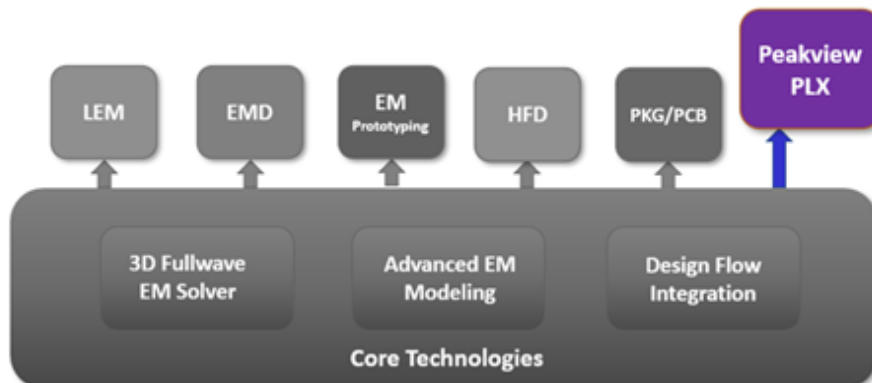
Standard Format Support

PLX Setup
iRCX or ITF files from foundries
LVS cleaned data with PEX results.

PLX Input
Calibre LVS® clean design
PEX: Calibre xRC®/Synopsis StarRC™/Cadence® QRC results in DSPF

PLX Output
DSPF file, ready for circuit simulation

Platform
Linux 64-bit, i.e., Red Hat and SUSE
LSF/NC-based computing farm