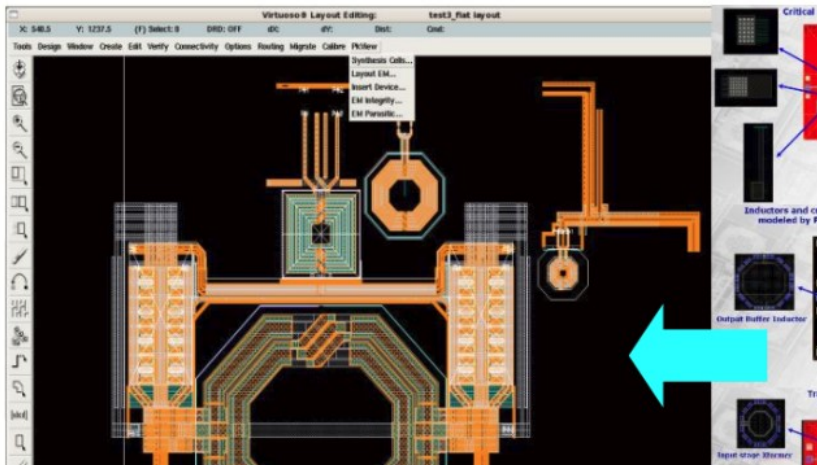


Overview

PeakView's LEM™ is a powerful yet easy to use, 3D Fullwave EM modeling solution. It can be operated as standalone or from within Virtuoso® or Custom Compiler™ design environment with a simple click of button for passive device and interconnect structures to be automatically extracted for a complete 3D electromagnetic analysis. PeakView's new powerful high-capacity EM solver (HCS) supports volume meshing of the most challenging device and multi-port structures such as MIMCAP and interconnects and accounts for multi-sheet currents and sidewall capacitance to produce silicon accurate EM models with corresponding design views for the selected library. LEM™ provides a versatile user interface and enables designers to incrementally adjust the parameters of devices throughout design. Composite layouts with passives, interconnects, DFM structures (e.g. fill) and wafer scale package elements can be EM analyzed together. The state-of-the-art electromagnetic simulation technology provides the performance, capacity and accuracy for meeting today's most stringent electromagnetic IC design needs from DC-mmWave-TeraHz for ultra broadband spectrum.



Features

Advanced EM Modeling

1. Support for Advanced Processes

LEM™ is process independent hence supports from mature node down to 3nm, it addresses the sub-40nm challenges in advanced processes with the PeakView™ chemical-mechanical polishing (CMP) option. This feature allows LEM™ to accurately simulate and model complex metal slotting, striping, and via arrays, aiding time-efficient automated design. It provides comprehensive modeling methods for dummy metal fill with passive devices over all frequency ranges.

PeakView LEM™, in conjunction with CMP™, provides full support for advanced process node DFM requirements during EM synthesis and Layout EM extraction. Designers are able to define their own metal fill and slotting requirements in the PCircuit parameters. During EM synthesis, these rules are considered and PeakView delivers a DRC clean layout with accurate EM and circuit simulation models.

2. Physics-Based Modeling

In addition to purely numerical n-port S-parameter models, LEM™ also provides the option to generate compact RLCK models called Physics-Based Models (PBM) that guarantees passivity and physical reliability. PBM generates

Benefits

Support Advanced Process Nodes & Technologies

support for advanced process nodes from 65nm to 3nm PDKs with the most up-to-date design rules and utilities (i.e. metal-fill). PeakView's iRCX and ITF Parsers simplify importing PDK layer process information into the tool. All process nodes with any metal stack-up are supported in LEM™.

Design Flow Support

LEM™ is seamlessly integrated into the Virtuoso® and Custom Compiler™ layout editors with a bi-directional, lossless data exchange interface. Designers are able to utilize the tool in their familiar IC design environment.

Accuracy, Capacity & Performance

PeakView's patented EM solver combines high accuracy, computational performance and capacity needed to analyze complex layouts with devices, interconnect and Packaging and 3D-IC interfaces. It matches silicon accuracy and supports frequencies from DC – mmWave – Terahertz range.

Automated Layout Processing

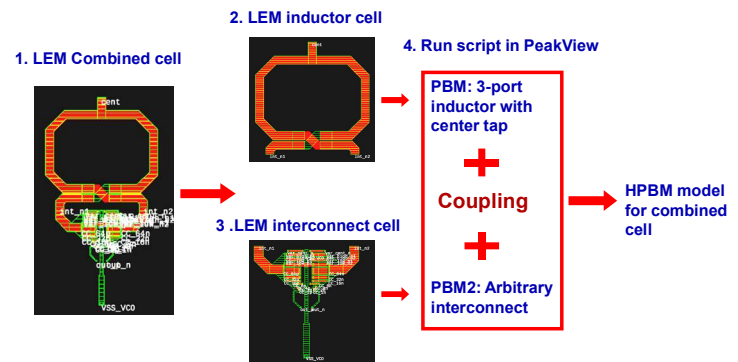
PeakView™ automatically processes compound designs and generates corresponding layouts for EM simulation. The layouts are algorithmically verified and modeled; users are not required to make any modification (e.g. simplifying via, metal fill etc.) to their designs. With automated internal layout processing, PeakView™ LEM

EM models as Spectre or HSPICE equivalent sub-circuits for use in transient simulations. PBM models are guaranteed to be convergent and passive over a user selectable frequency range. PBM preserves the DC inductance, resistance and does not shift the circuit's operating point. In addition, PeakView PBM automatically ensures that the model correctly accounts for white noise content.

Interconnect with irregular or non-uniform structures can also be modeled with 2nd generation Physics-based Models (PBM2). PBM2-based LEM is able to convert S-parameter models of arbitrary geometries with high port counts into compact equivalent circuit models that can be used in time-domain circuit simulations. This enables designers to easily perform transient simulations of their designs with EM-level accuracy. Finally the latest Hierarchical PBM (HPBM) also accounts for the inductive and capacitive coupling effects among devices.

3. Hierarchical PBM

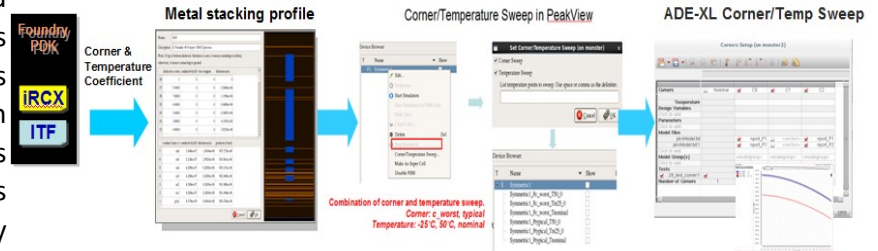
PeakView™ Hierarchical PBM (HPBM) solution is an elegant strategy to model the combined EM effects based on the individual contributing components, which could be the passive device, complex or interconnect structures. The HPBM has been developed to address the modeling of complicated structures by bringing in an innovative hierarchical view to the modeling process. In the HPBM flow, user can specify different PBM methods for each sub-component. PeakView will then produce a single PBM model of the entire design by combining the sub-component models and adding coupling effects between them.



Tool Integration

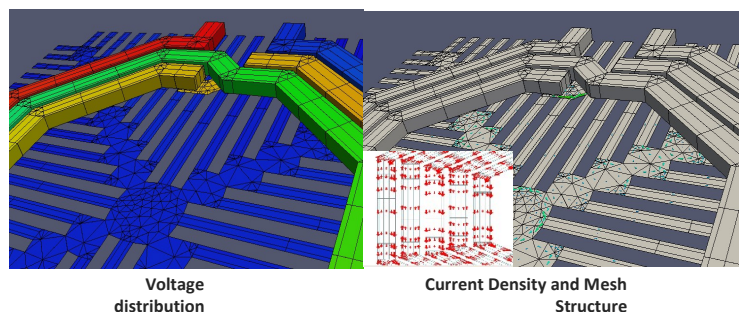
1. Process Corner and Temperature Coefficient Modeling

PeakView™ generates S-parameter and lumped models that account for process corner and temperature sweeps. Foundries provide several types of technology files in terms of Rbest, Rworst etc., that reflects process variations. Temperature coefficients of materials are also obtained from technology files. PeakView™ generated corner based model files accounting for process corners and temperature coefficient analysis and can be synced to the design library. The models can be utilized within popular simulation environments such as ADE-XL.



2. Visualization

PeakView LEM's visualization system expedites debugging of device design by showing the EM mesh, voltages, currents and charge distribution. Inaccuracies in the structures are apparent early and can be fixed preemptively in the design phase. The built-in visualization window provides for better understanding of skin effects and capacitive coupling, image currents at various frequencies. The chart window plots pre-defined and user-defined quantities of interest from EM simulation results.



Voltage and charge visualization LEM simulations are shown in the above figure.

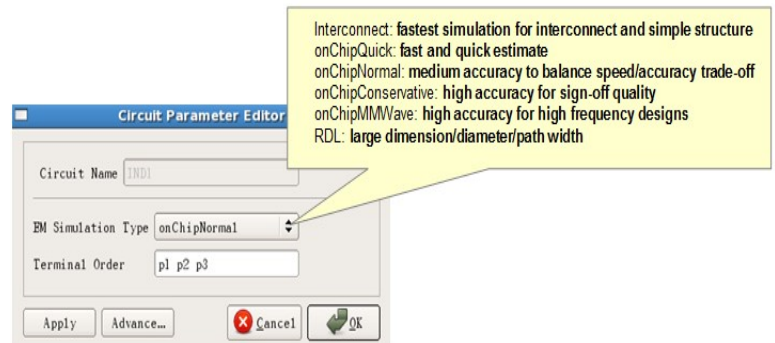
3. Support Backward Compatibility with Legacy Layouts

PeakView LEM™ supports legacy designs containing devices that are not synthesized with PeakView™ or that were created with Virtuoso® prior to use of PeakView™. After EM extraction with LEM™, the S-parameter and circuit models of each device are generated. PeakView™ prepares models for Cadence Spectre RF and HSPICE simulations.

High-Performance Features

1. Customized Accuracy Types Just a Button Away

In addition to pre-configured EM simulation types, PeakView™ has implemented Pre-Customized Accuracy Types to enhance the flexibility of accuracy settings and to configure layout processing and EM simulation options. By composing a configuration file, users can easily tailor the tool such that the entire EM simulation process is optimized for special design structure requirements. This is particularly useful for scenarios where concurrent simulation for structures of varying scales is required.



2. Multi-core Processing and Distributed Computing

To maximize utilization of computing resources, LEM™ takes advantage of PeakView's multi-core processing capability. Design jobs can be run on multi-core machines and standalone platforms with multi-processor hardware to maximize computing efficiency. Users can also specify different frequency points to be simulated on different machines in a compute farm.

3. A Revolutionary EM Solver Technology

New Direct Solver Engine:

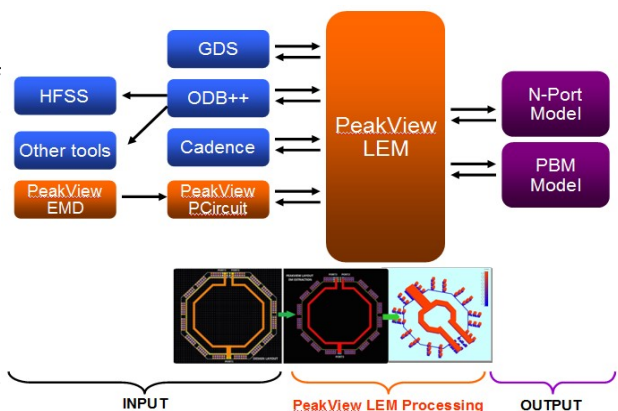
- Quick EM technology to drastically boost simulation performance without the loss of accuracy.
- Added GPU and CPU/GPU performance enhancements capability.

Iterative High Capacity Solver (HCS):

- 5 to 30x memory reduction while maintaining within 1% accuracy of 3D full-wave direct solver accuracy.
- Ideal for large scale EM simulations, such as metal fill, full chip, IC-Pkg-PCB and 3D-IC Co-simulation.

LEM™ Flow

The PeakView LEM™ flow accommodates three different modeling approaches frequently used by designers. For Layout EM analysis users can: **1.** launch LEM™ from within their Virtuoso® environment and export their layouts to PeakView™, **2.** Import a GDSII format layout file into PeakView™ or, **3.** Synthesize a layout in PeakView™ using PCircuits. Design layouts that contain compound structures of varying scales (on-chip devices, large RDL lines, PCBs, planar package elements) and contours (polygons of any angles, circular via holes, curved paths) are accurately processed by LEM™. LEM™ generates a corresponding layout in the PeakView™ GUI. PeakView's high precision EM engine is then used to electromagnetically analyze the layout and create relevant views corresponding to the EM models. Generated views are then synced to the Virtuoso® Library to be used for SPICE simulation.



Applications

LEM™ is useful for a wide variety of applications in semiconductor design. LEM, based on PeakView™ high precision, 3D EM solver, performs accurate signal integrity analysis on complex layouts consisting of a broad class of elements. LEM™ efficiently characterizes broadband (e.g. clock-lines), as well as narrowband (e.g. LNAs) applications, from DC to mmWave to THz spectrum. Applications include, but are not limited to:

Passive Devices

Inductors, MOM cap, MIM cap, baluns, transformers and commonly used device topologies and associated metal fill, guard-rings, patterned ground shields, etc.

Interconnect

Microstrip lines, co-planar waveguide (CPW) lines, T and X junctions and other planar transmission signal routing

DFM Structures

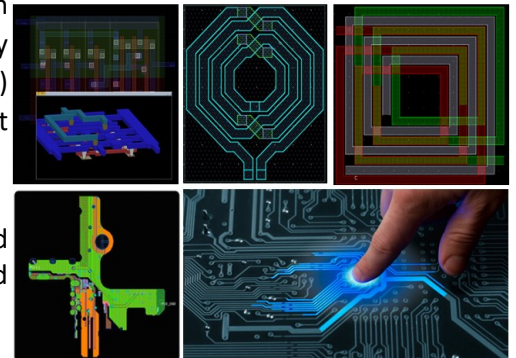
Metal fill, wide-metal slotting, striping in advanced process nodes (20nm and beyond)

Board-level Analysis

PCB coupling effects e.g. sensor placement in board-level analysis, feedback impedance return path via ground plane

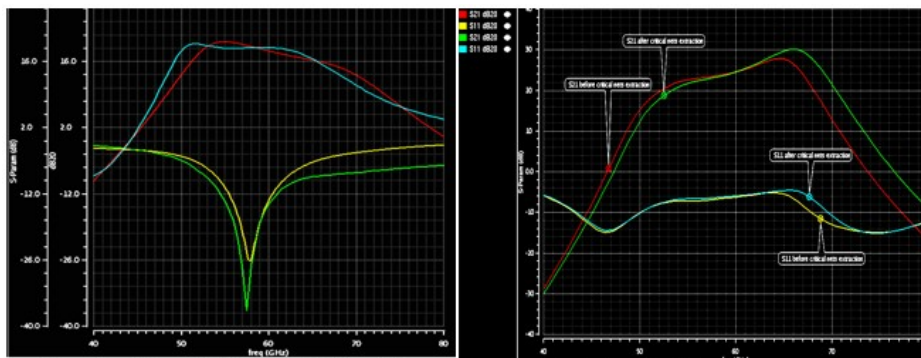
Wafer-Scale Package Elements

Coupling between planar wafer-scale package elements and on-chip passives



Silicon Data Correlation

PeakView LEM™ simplifies the process of complex system-level EM design, and offers sign-off quality that is benchmarked with measurements. Our products are seamlessly integrated into the IC design environment to support the most advanced process nodes such as 3nm, thereby greatly eases the steps for EM design with high confidence. PeakView™ EM modeling solutions continue to demonstrate excellent correlation to silicon data. Our EM design flows have been demonstrated in TSMC RF Reference Design Kits and test-keys, simulation and measurement



a. Silicon Correlations at 60 GHz for PeakView™ Transmission Line Models for a PA Module

b. closely matched circuit simulation and silicon measurements for a 60GHz low-noise amplifier (LNA) using PeakView™ transmission line and inductor models.

results correlation for PA and LNA designs at 60 GHz using PeakView™ Transmission Line Models for TSMC 65nm and below. Then at TSMC 20nm process, PeakView™ simulations of inductors with a variety of metal fill shapes and densities were compared to measurements. The result indicated a close match of silicon measurement for bottom plate capacitance when PeakView CMP was used for metal fill modeling.

Standard Format Support

LEM Setup

- iRCX format technology file from TSMC
- ITF format technology file from foundries

LEM Input

- Virtuoso® or Laker™ layout with pins
- GDSII Layout
- PCircuit

LEM Output

- n-port, Physics-Based EM models.
- Model views added to Cadence® Library.

Platform

Linux 64-bit, i.e. Red Hat and SUSE