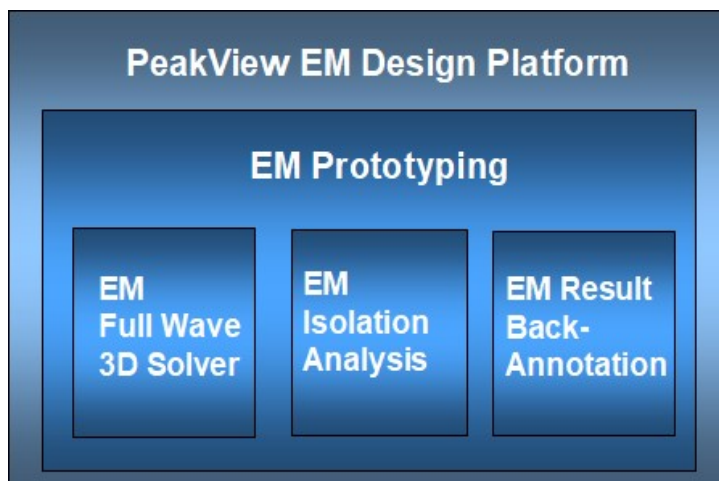


Overview

PeakView EM Prototyping tool addresses the capability of circuit-level EM isolation, coupling and crosstalk simulation at early stage of the millimeter wave chip development cycle while the layout and perspective EM devices placement and connectivity is still under development and not reached the state of LVS clean nor completion. In other words, throughout any phase of the design cycle, the millimeter wave IC design team may begin to evaluate the physical EM effects of crosstalk and coupling among EM devices and/or the interconnects maybe accurately evaluated through EM isolation, full-wave EM simulation and modeling to determine and gauge if the coupling effects could introduce any detrimental effects on the overall circuit performance. Such EM prototyping process requires the layout preparation of multiple EM devices for simulation, modeling and back-annotation while preserving the connectivity throughout the design hierarchy. PeakView EM Prototyping tool allows this type of complex EM simulation, modeling and perspective analysis done seamlessly and automatically.



Key Underlying Technologies:

- 3D Full-Wave EM Solver ensures accuracy from DC to Terahertz frequency range.
- Circuit-level EM isolation, coupling and crosstalk modeling throughout design stages.
- Full EM model and HPBM back annotation to hierarchical top cell schematic test bench

Benefits

DC to Terahertz Accuracy & Performance

PeakView's 3D Full-Wave EM Solver provides the complete solution of the full Maxwell Equations for solving any specific EM problem. 3D accuracy is much more advanced than the 2.5D and planar-3D accuracy. Traditionally 2.5D EM assumes the conductor is infinitely thin, which may be a good assumption for early-days mmWave circuits (microstrip line, etc). Planar-3D EM addresses thickness without volume meshing, while 3D EM needs to compute the 3D structure accurately with full 3D meshing. This becomes critical for contemporary high-speed circuits at high frequencies that stretches to Terahertz frequency range.

Automation and Flow Integration

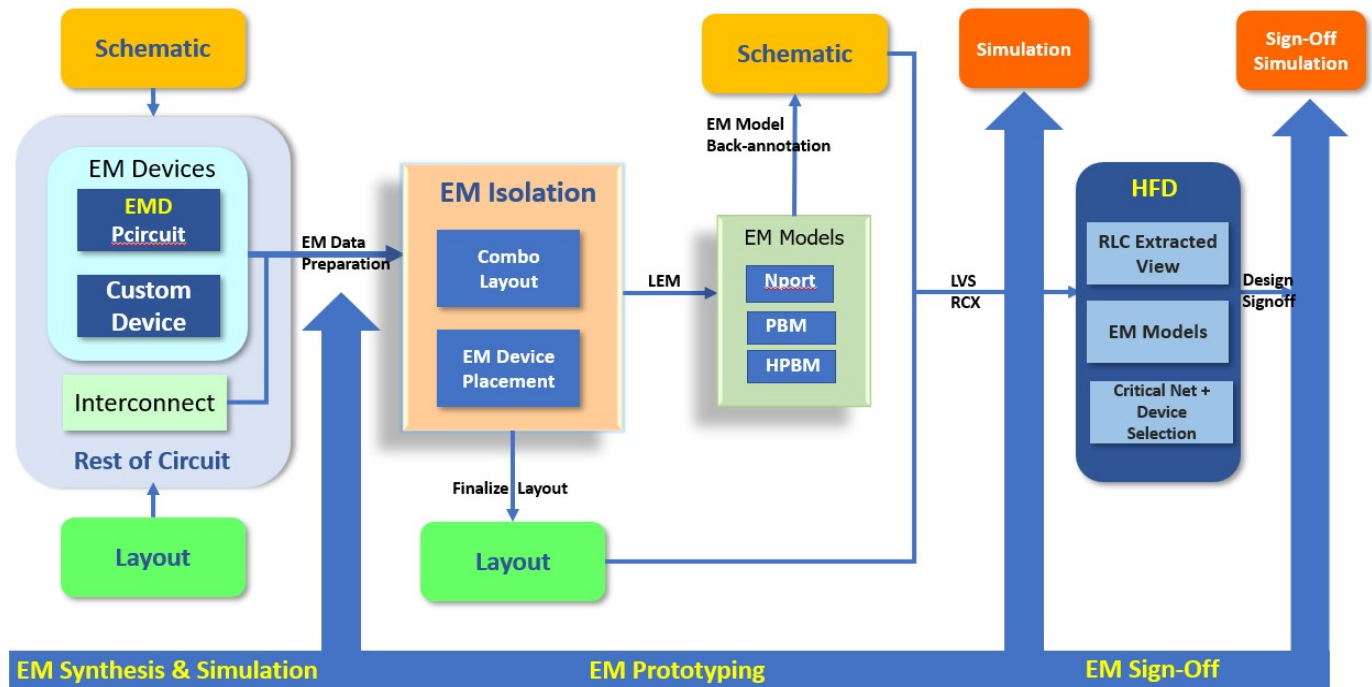
PeakView EM Prototyping is integrated into Virtuoso® schematic and layout along with the use of hierarchy editor to preserve EM and corresponding design hierarchy. This enables designers to work within a familiar IC design environment. Designers can work with the top cell test bench in schematic and layout even before LVS and layout completion. EM Prototyping then prepares combo cell for EM isolation and analysis, model generation and back-annotation. It manages all the details behind the scenes and automatically ensures design data integrity while including the EM effects in the circuit simulations.

Wide Applications

PeakView EM Prototyping places special emphasis on electromagnetic coupling effects present in a wide range of RFIC and transmission media. In addition, it excels in performing circuit level analysis of EM device and interconnect interactions throughout different stages of design cycle, with the aid of EM isolation technique, PeakView is capable of capturing noise floor down to -130db. The process will aid the optimal planning and placement of EM devices to avoid detrimental impacts on overall system performance in designs such as (VCO), low-noise amplifiers (LNA), power amplifiers (PA), differential transmission lines, CPW lines, micro-strip lines, digital clock lines and a host of other millimeter-wave designs.

PeakView's Complete EM Solution from Prototyping to Sign-Off

Today's compact millimeter wave design requires rigorous analysis of the interaction between EM devices to avoid the degradation of performance to the system. While such type of EM analysis needs to be performed at any stage of the design cycle to avoid costly design re-spin.



The EM Prototyping tool along with HFD complements PeakView's coverage on the high frequency EM analysis of chip design from prototyping to sign off.

- The EM Prototyping tool enables the study of the behavior of the chip at early stage of the layout process while multiple layouts are not yet complete nor LVS clean.
- HFD analyzes the high frequency effects of critical interconnect and devices from the RLC parasitic elements perspective at a later stage of the design when the layout is LVS-clean.

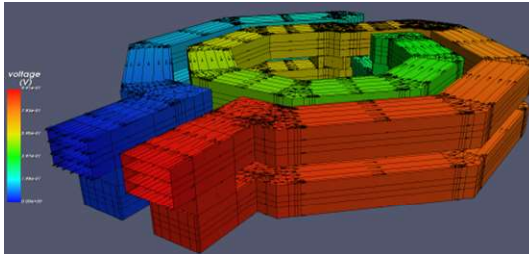
HFD has been benchmarked by our high-frequency, RF and mixed-signal IC design customers to be the most reliable and efficient electromagnetic extraction tool to date. It is also emerging as a revolutionary millimeter wave technology aiding in the design and verification of broadband gigabits per second (Gbps) on-chip wireless systems. Full-scale implementation of this technology will greatly facilitate research and development in the 5G (5th Generation wireless network) standards and associated hardware, where millimeter wave frequency bands are of primary interest.

3D Full-Wave EM Solver Accuracy

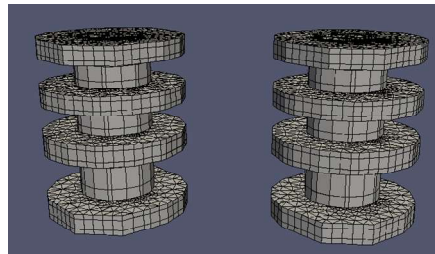
PeakView's 3D Full-Wave EM Solver can compute the 3D structure accurately by performing full 3D meshing. PeakView Solver adopts volume meshing with multi-sheet current calculation, along with vertical inductance, resistance and side wall capacitance calculation. All these become critical for contemporary high-speed circuits at high frequencies that stretches all the way to Terahertz frequency range (> 200Gz). In terms of capacity,

PeakView engine also offers the iterative High-Capacity Solver (HCS) technology which represents a major breakthrough in memory reduction by 5 to 30 times, hence capable of large solving capacity while maintaining the full-wave accuracy.

Volume Meshing

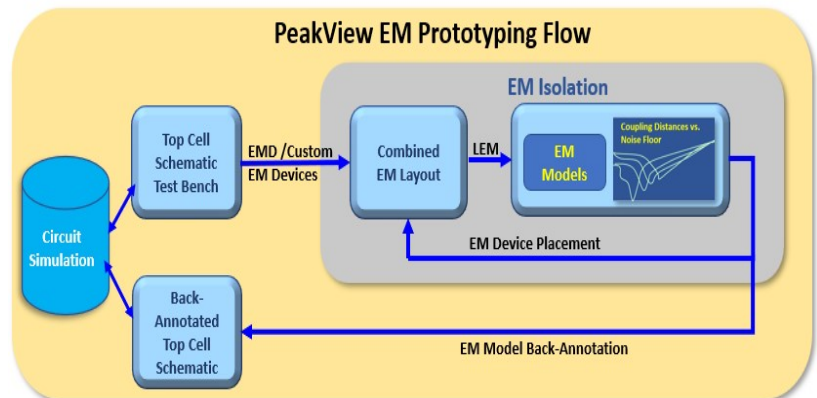


Vertical Inductance Meshing

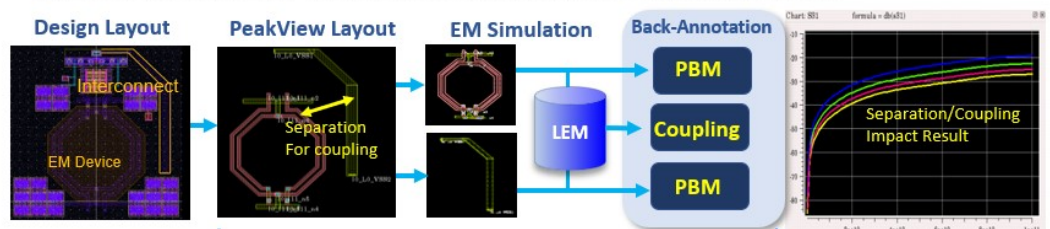


EM Prototyping Flow with EM Isolation

User initiates the “PeakView EM Prototyping” tool from the top cell schematic Test Bench. PeakView creates a scratch layout with the recognized EM devices (Inductors, transformers, T-Coils, etc) as a combined cell. The user may then perform layout modification and placement of the EM devices. All EM devices may now be loaded to PeakView for EM simulation through the combined layout where the coupling effects and noise floor can be studied accordingly. Finally, the nport and HPBM results can be back annotated to the top cell schematic Test Bench to exam the overall effect on the design performance. The EM Prototyping flow not only models coupling effects between EM devices but can also be used to analyze the coupling effects between EM devices and interconnects such as power line...etc. For an example, if the combined cell become EM device + Interconnect, where the effect can be adjusted by varying the distance between the power-line(Interconnect) and the transformer (EM device).

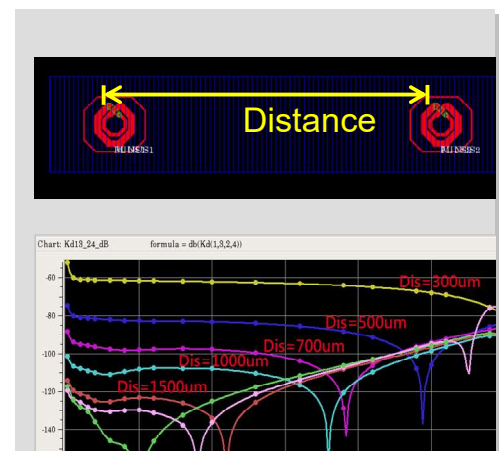


EM Prototyping: Device & Interconnect Coupling on Design Performance



EM Isolation

EM isolation analysis is a specialized field of EM simulation, which focus on the EM design and simulation techniques related to couplings and isolations. For modern RF and 5G SOC designs, EM isolation analysis is essential and critical for sensitive and elusive high speed circuits to ensure design success. Traditional parasitic extractions do not have the full-wave frequency accuracy for the detailed remote coupling analysis under EM Isolation scenario, hence the traditional EM tools are not well developed nor qualified for EM Isolation analysis to capture the targeted EM isolation noise floor.

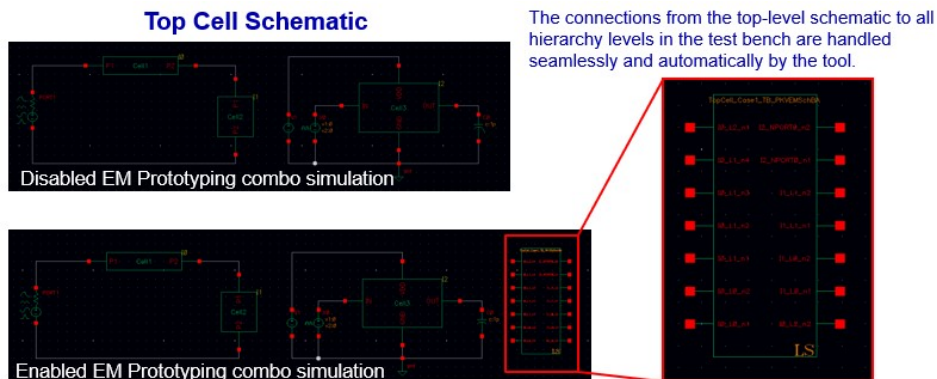


EM isolation noise floor defines the lowest coupling value that EM tools can capture without losing numerical accuracy or physical meaning. Today, PeakView is capable of handling severe EM Isolation Analysis needs: It achieves -110dB for the EM isolation noise floor with HCS and flat engine, and -130dB as the maximum EM isolation noise floor. EM isolation is the ratio of mutual term over self term to measure the coupling effects relative to the source of couplings.

EM Isolation analysis is also aided by built-in formula, post-processing and visualization/animation features. Example: EM Isolation design techniques can be explored through increasing the design distance, guard rings, grounding structures, patterned ground shields, and NTN/BFMOAT process structures.

Powerful Schematic Back-Annotation of EM Results

PeakView will automatically incorporate EM simulated (nport /lumped model) results back into specific locations of the top-cell schematic via the smart backannotation of the combo EM results through the insertion of the combo symbol (`_PKVEMSchBA`) into the top cell schematic. Without the smart backannotation, user would have to manually break the schematic connections across various hierarchies and reconnect the EM model possibly with hundreds of pins. With our smart backannotation, we have achieved no change on the schematics across hierarchies. EM model connectivities in the circuit are maintained seamlessly and accurately across hierarchies.



PeakView EM Prototyping is very versatile yet powerful that can combine with other strong PeakView modeling capabilities such as HPBM to model and support the back-annotation of hierarchical based PBM (Physics Based Models) which may contains the individual PBM models of EM devices to the affected interconnect models and the coupling effects between them throughout the design hierarchy.

Standard Format Support

EM Prototyping Setup

- iRCX format technology file from TSMC
- ITF format technology file from foundries

EM Prototyping Input

- Virtuoso® or Custom Compiler™ Schematic or layout with pins
- GDSII Layout
- PCircuit

EM Prototyping Output

- n-port, Physics-Based EM models.
- Model views added to Cadence® Library.

Platform

Linux 64-bit, i.e., Red Hat and SUSE
LSF/NC-based computing farm.