

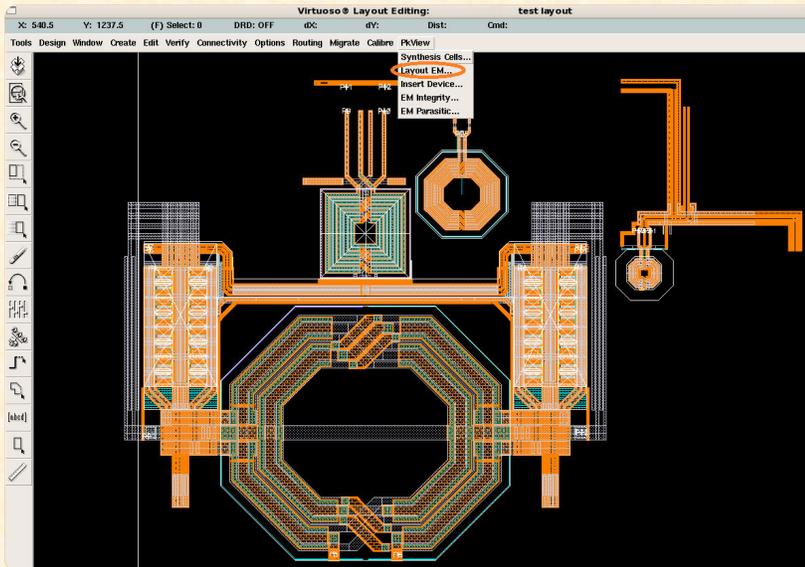
# PeakView Layout EM (LEM)

## Overview

PeakView's LEM™ solution provides users with a fast, easy to use, 3D EM modeling capability from within their design environment. A single click from within the Virtuoso® or Laker™ layout views allows for designs with passive structures and interconnect to be automatically extracted for a complete 3D electromagnetic analysis. PeakView's high-capacity EM engine supports complex multi-port structures and swiftly creates accurate EM models with corresponding views in the design library.

LEM™ is a versatile, easy-to-use tool that supports electromagnetic analysis and modeling of design layouts. It enables designers to incrementally adjust the parameters of precisely architected devices during their design process. Composite layouts with passives, interconnect, DFM structures (e.g. fill) and wafer scale package elements are accurately EM analyzed with LEM.

The state-of-the-art electromagnetic technology provides unique benefits of fully automated design flow, fast simulation, accurate results, high capacity, advanced geometry processing and easy-to-use simulation settings that optimize users' electromagnetic IC design performance.



PeakView™ LEM for Layouts with Devices and Interconnect

## Benefits

### Support for Advanced Process Nodes and Technology

LEM™ provides support for advanced process nodes (i.e. 20nm, 16nm PDKs) with the most up-to-date design rules and utilities (i.e. metal-fill). PeakView's iRCX and ITF Parsers simplify importing PDK process information into the tool. All process nodes with any metal stack-up are supported in LEM™.

### Design Flow Integration

LEM™ is seamlessly integrated into the Virtuoso® and Laker™ layout editors with a bi-directional, lossless data exchange interface. Designers are able to utilize the tool in their familiar IC design environment.

### Accuracy, Performance and Capacity

PeakView's patented EM solver combines high accuracy, computational performance and the capacity needed to analyze complex layouts with devices, interconnect and PCB interfaces.

### Automates Layout Processing

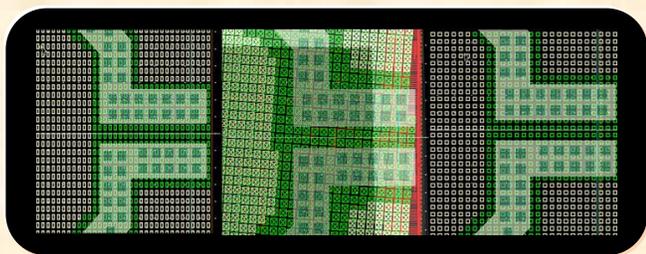
PeakView™ automatically processes compound designs and generates corresponding layouts for EM simulation. The layouts are algorithmically verified and modeled; users are not required to make any modification (e.g. simplifying via, metal fill etc.) to their designs. With automated internal layout processing, PeakView™ LEM generates signoff quality models with no loss in accuracy.

## Features

### ▪ Advanced EM Modeling Features

#### 1. Support for Advanced Processes

LEM™ addresses sub-40nm challenges in advanced processes with the PeakView™ chemical-mechanical polishing (CMP) option. This feature allows LEM™ to accurately simulate and model complex wide metal slotting, staggered slotting/stripping, and massive via arrays, aiding time-efficient automated design. It provides comprehensive modeling methods to enable users to accurately model dummy metal fill with passive devices over all frequency ranges.



Rectangular, auto and square fill in PeakView™

PeakView LEM™, in conjunction with CMP™, provides full support for advanced process node DFM requirements during EM synthesis and Layout EM extraction. Designers are able to define their own metal fill and slotting requirements in the PCircuit parameters. During EM synthesis these rules are considered and PeakView delivers a DRC clean layout with the industry's most accurate EM and circuit simulation models.

#### 2. Physics-Based Modeling

In addition to purely numerical n-port S-parameter models, LEM™ also provides the option to generate compact RLCK models called Physics-Based Models (PBM) that guarantee passivity and physical realizability. PBM generates EM models as Spectre or HSPIICE compatible equivalent sub-circuits for use in transient circuit simulations. PBM models are guaranteed to be convergent and passive over a user selectable frequency range. PBM preserves the DC inductance and resistance, and does not shift the circuit's operating point. In addition, PeakView PBM automatically ensures

that the model correctly accounts for white noise content.

Interconnect with irregular or non-uniform structures can also be modeled with Physics-based Models (PBM2). PBM-based LEM is able to convert S-parameter models of arbitrary geometries with high port counts into compact equivalent circuit models that can be used in time-domain circuit simulations. Combining LEM with HFD for EM integrity analysis on coupling groups makes it easier to detect and repair EM integrity issues at circuit level. This enables designers to easily perform transient simulations of their designs with EM-level accuracy.

#### 3. Hierarchical EM

PeakView™ Hierarchical Electromagnetic (HEM) solution is an elegant strategy for reduction of computational complexity to yield a faster simulation time than a flat-mode solver. The HEM engine uses a divide and conquer algorithm to partition a large problem into smaller counterparts. With the aid of parallel processing, the smaller geometries are first solved quickly. The partial solutions are then iteratively combined into a final solution of the original problem by computing the global coupling effects among the sub-components.

### ▪ Tool Integration

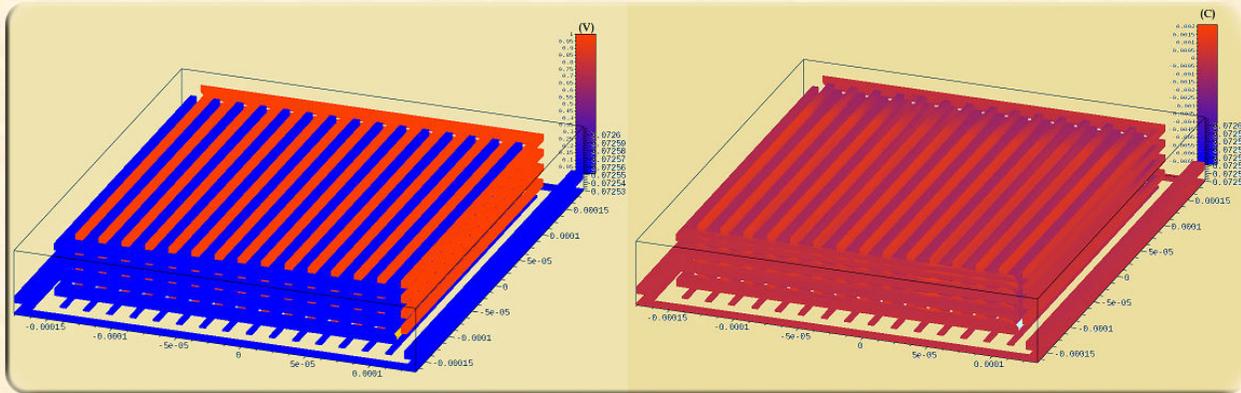
#### 1. Process Corner and Temperature Coefficient Modeling

PeakView™ generates S-parameter and lumped models that account for process corner and temperature sweeps. Foundries provide several types of technology files in terms of Rbest, Rworst etc., that reflect process variation. Temperature coefficients of materials are also obtained from technology files. PeakView™ generated cell-views accounting for process corner and temperature coefficient analysis models are synced to the design library. The models can be selected for circuit simulation using the Cadence® Hierarchy Editor.

## 2. Design Visualization and Chart Window

PeakView LEM's visualization system expedites debugging of device design by showing the EM mesh, voltages, currents and charge distribution. Inaccuracies in the structures are apparent early and can be fixed preemptively in the design phase. The built-in visualization window provides for better understanding of skin effects and capacitive coupling, image currents at various frequencies. The chart window plots pre-defined and user-defined quantities of interest from EM simulation results.

Voltage and charge visualization LEM simulations are shown in the following figure.



Voltage and Charge Distribution Visualization in PeakView™

## 3. Backward Compatibility with Layout Editors

PeakView LEM™ supports legacy designs containing devices that are not synthesized with Peakview™ or that were created with Virtuoso® prior to use of PeakView™. After EM extraction with LEM™, the S-parameter and circuit models of each device are generated. PeakView™ prepares models for Cadence Spectre RF and HSPICE simulations.

### ▪ High-Performance Features

#### 1. Customized Accuracy Types

In addition to pre-configured EM simulation types, PeakView™ has implemented Customized Accuracy Type to enhance the flexibility of accuracy settings and to configure layout processing and EM simulation options. By composing a configuration file, users are able to easily tune the tool such that the entire EM simulation process is optimized for special test cases. This is particularly useful for scenarios where concurrent simulation for structures of varying scales is required.

#### 2. Multi-core Processing and Distributed Computing

In order to maximize utilization of computing resources, LEM™ takes advantage of PeakView's multi-core processing capability. Design jobs can be run on compute farms consisting of multi-core machines, as well as on standalone platforms with multi-processor hardware to achieve maximum efficiency of computing resources. PeakView provides different distributed computing modes to concurrently accelerate the EM modeling. Users are able to specify different frequency points to be simulated on different machines in a compute farm.

#### 3. Hybrid Matrix Decomposition Technology

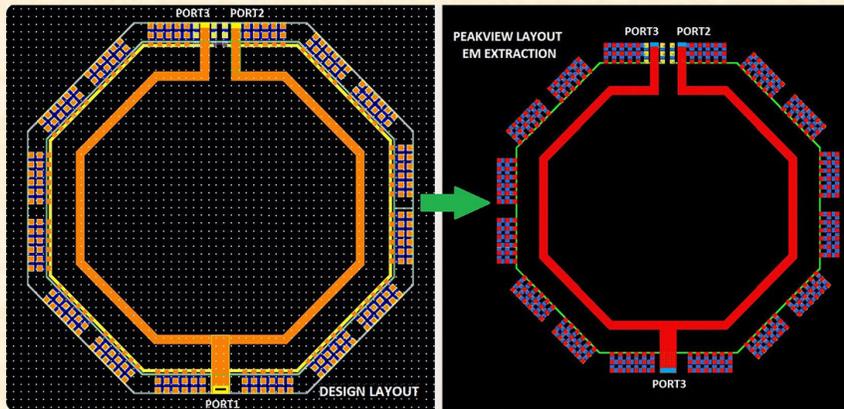
PeakView™ has developed a hybrid matrix decomposition technology to achieve rapid solutions for both DC and EM simulation. A set of advanced mathematical methods which combines the advantageous aspects of sparse matrix and dense matrix solution technologies has been implemented in

the engine. The overall simulation time is now greatly minimized with the new developments in matrix decomposition methodology.

### LEM Flow

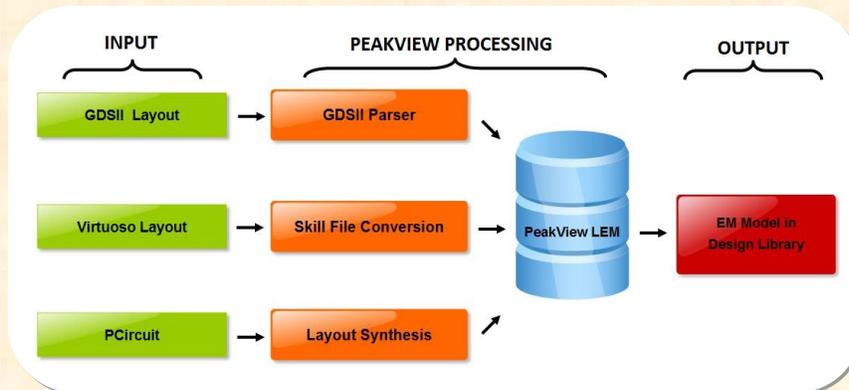
The PeakView LEM™ flow accommodates three different modeling approaches frequently used by designers. For Layout EM analysis users can: **1.** launch LEM™ from within their Virtuoso® environment and export their layouts to PeakView™, **2.** Import a GDSII format layout file into PeakView™ or, **3.** Synthesize a layout in PeakView™ using PCircuits.

Design layouts that contain compound structures of varying scales (on-chip devices, large RDL lines, PCBs, planar package elements) and contours (polygons of any angles, circular via holes, curved paths) are accurately processed by LEM™.



Virtuoso® Layout EM Extraction (Courtesy of TSMC RDK 3.0)

LEM™ generates a corresponding layout in the PeakView™ GUI. PeakView’s high precision EM engine is then used to electromagnetically analyze the layout and create relevant views corresponding to the EM models. Generated views are then synced to the Virtuoso® Library to be used for SPICE simulation.



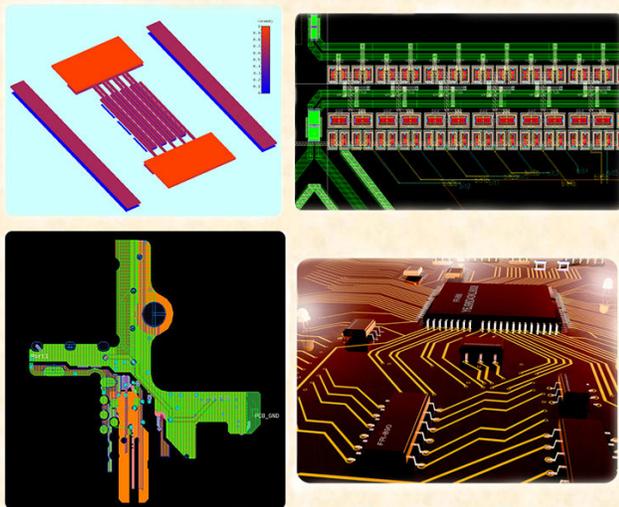
LEM Flow

### Applications

LEM™ is useful for a wide variety of applications in semiconductor design. LEM, based on PeakView™ high precision, 3D EM solver, performs accurate signal integrity analysis on complex layouts consisting of a broad class of elements. LEM™ efficiently characterizes broadband (e.g. clock-

lines), as well as narrowband (e.g. LNAs) applications, from DC to the sub-THz spectrum.

Applications include, but are not limited to:



LEM Applications

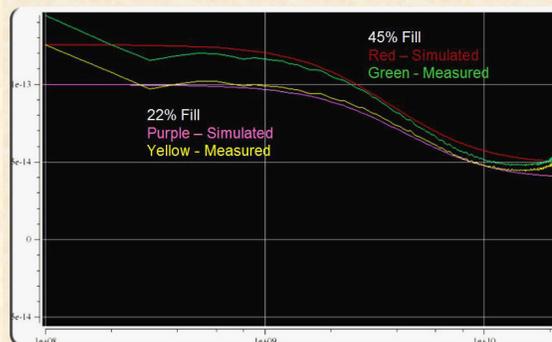
- **Passive Devices**  
Inductors, MOM capacitors, MIM capacitors, baluns, transformers and commonly used device topologies and associated metal fill, guard-rings, patterned ground shields etc.
- **Interconnect**  
Microstrip lines, co-planar waveguide (CPW) lines, T and X junctions and other planar transmission media or signal routing
- **DFM Structures**  
Metal fill, wide-metal slotting, striping in advanced process nodes (20nm and beyond)
- **Board-level Analysis**  
PCB coupling effects (e.g. sensor placement for board-level analysis, feedback impedance return path via ground planes)
- **Wafer-Scale Package Elements**  
Coupling between planar wafer-scale package elements and on-chip passives

## Silicon Data Correlation

PeakView LEM™ simulations confirm excellent correlation with silicon data in advanced process nodes. It is capable of modeling dense, detailed structures. For instance, the simulation

engine has a special feature: onchipFingerCap, which is designed to optimize the EM simulation efficiency for finger cap structures. Finger caps are usually constructed with small metal spacing and high densities. PeakView™ profile setup carefully considers the width, spacing and sheet resistance variation tables from the foundry. By correctly accounting for layout dependent effects, it produces a close match between EM simulation results and silicon data to ensure first-pass silicon success.

PeakView LEM™ results have been validated using silicon data for metal-fill modeling in TSMC's 20nm process. PeakView simulations of 20nm inductors with a variety of fill shapes and densities were compared to de-embedded test chip measurements. The following figure shows a close match of simulation results vs. measurement for bottom plate capacitance when PeakView CMP was used for fill modeling.



Simulation vs. Measurement in TSMC 20nm Process

## Formats

- **LEM Setup**
  - iRCX format technology file from TSMC
  - ITF format technology file from foundries
- **LEM Input**
  - Virtuoso® or Laker™ layout with pins
  - GDSII Layout
  - PCircuit
- **LEM Output**
  - n-port, Physics-Based EM models.
  - Model views added to Cadence® Library.
- **Platform**
  - Linux 64 bit, i.e. Redhat and SUSE
  - LSF-based computing farm